REMARKS

By this Amendment, Applicant amends claims 2, 7 and 9 to correct minor typographical errors. Accordingly, claims 1-16 remain pending in the application.

Applicant acknowledges the indication that claim 4, 6, 10, 12, 14 and 16 define allowable subject matter and would be allowed if rewritten in independent form to include all limitations of their respective base claims, and any intervening claims.

Reexamination and reconsideration of the application are respectfully requested in view of the following Remarks.

35 U.S.C. § 102

The Office Action rejects claim 1-3, 5, 7-9, 11, 13 and 15 under 35 U.S.C. § 102 over Blanc et al. U.S. Patent 6,606,300 ("Blanc").

Applicant respectfully traverses these rejections for at least the following reasons.

Claim 1

Among other things, the data pipeline circuit of claim 1 includes a control signal generating unit adapted to receive a clock signal and adapted to output a control signal, a first switching signal, and a second switching signal, according to a frequency of the clock signal.

Applicant respectfully submits that Blanc does not disclose a data pipeline circuit as recited in claim 1 including a control signal generating unit adapted to receive a clock signal and adapted to output a control signal, a first switching signal, and a second switching signal, according to a frequency of the clock signal.

The Office Action confusingly jumps back and forth[1] between various portions of Blanc, picking and hunting for various elements of claim 1 to somehow try to

[1] In its discussion of claim 1 alone, the Office Action jumps – in order – from col. 4, to col. 2, to col. 37, to col. 35, back to col. 4, to col. 14, and then to col. 38 – not even counting the various references to unspecified "Associated text" for: FIGs. 2, 3, 11; FIGs. 1-5, 11 and 21; FIG. 6. Applicant respectfully submit that the Office Action does not fairly put Applicant ion notice as to how exactly it is believed that Blanc supposedly discloses the elements of claim 1. A simple citation to reference numerals would have been more fruitful to advancing prosecution of this application.

cobble together the complete data pipeline circuit as recited in claim 1. However, as best as Applicant can understand the Office Action, it appears that the Office Action is asserting that the phase acquisition circuit 7212-j of FIG. 22A (ironically, one of the figures that is **not** specifically cited in the Office Action!) corresponds to the control signal generating circuit of claim 1.

Applicant respectfully submits that Blanc does not disclose the control signal generating circuit of claim 1, and more specifically, Applicant respectfully submits that the phase acquisition circuit 7212-j of FIG. 22A of Blanc cannot correspond to the control signal generating circuit of claim 1.

The control signal generating circuit of claim 1 outputs three signals: a control signal, a first switching signal, and a second switching signal.

The Office Action fails to even allege that the phase acquisition circuit 7212-j of FIG. 22A of Blanc outputs three signals: a control signal, a first switching signal, and a second switching signal. Instead, the Office Action only states that the phase acquisition circuit 7212-j outputs the first and second switching signals. And with good reason – clear inspection of FIG. 22A shows that the phase acquisition circuit 7212-j only outputs two clock signals.7216-j and 7217-j, and it does not output any separate control signal. Similarly, the cited text at col. 37, lines 22-28 only mentions the two clock signals.7216-j and 7217-j, and it does not mention outputting any separate control signal.

Therefore, for at least these reasons, it is not possible for phase acquisition circuit 7212-j of FIG. 22A of Blanc to correspond to the control signal generating circuit of claim 1.

Accordingly, for at least these reasons (and so many more!), Applicant respectfully submits that claim 1 is clearly patentable over Blanc.

Claims 2-3 and 5

Claims 2-3 and 5 depend from claim 1 and are deemed patentable over Blanc for at least the reasons set forth above with respect to claim 1.

Claim 7

Among other things, the device of claim 7 includes a control signal generating unit which is adapted to receive a first clock signal and a second clock signal, and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal.

Applicant respectfully submits that Blanc does not disclose a device as recited in claim 7 including a control signal generating unit which is adapted to receive a first clock signal and a second clock signal, and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal.

The Office Action does not specifically cite anything as allegedly corresponding to the control signal generating unit of claim 7. Instead, the Office Action very generally says: *"See rejection of claim 1 above."*

Unfortunately, claim 1 does not recite a control signal generating unit which is adapted to receive a first clock signal and a second clock signal, and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal.

In particular, Applicant respectfully submits that the phase acquisition circuit 7212-j of FIG. 22A of Blanc cannot correspond to the control signal generating unit of claim 7 because: (1) it does not receive first and second clock signals; and (2) it does not output a control signal.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 7 is clearly patentable over Blanc.

Claims 8-9 and 11-13

Claims 8-9 and 11-13 depend from claim 7 and are deemed patentable over Blanc for at least the reasons set forth above with respect to claim 7.

Claim 15

Among other things, the device of claim 15 includes a control signal generating unit adapted to receive a first clock signal, a second clock signal, and information about operation modes of the semiconductor memory device, and which is adapted to output a first switching signal, a second switching signal, and a control signal corresponding to the first clock signal, the second clock signal, and information about the operation modes of the semiconductor memory device.

The Office Action does not specifically cite anything as allegedly corresponding to the control signal generating unit of claim 15.

In particular, Applicant respectfully submits that the phase acquisition circuit 7212-j of FIG. 22A of Blanc cannot correspond to the control signal generating unit of claim 15 because: (1) it does not receive first and second clock signals; (2) it does not receive information about operation modes of the semiconductor memory device; and (3) it does not output a control signal.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 15 is clearly patentable over Blanc.

Claim 16

Claim 16 depends from claim 15 and is deemed patentable over Blanc for at least the reasons set forth above with respect to claim 15.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-16, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. §

1.17, particularly extension of time fees.

Respectfully submitted,

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